

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
)
Shunpei YAMAZAKI et al.)
)
Serial No.: 10/757,193)
)
Filed: January 14, 2004)
)
For: Method For Manufacturing Resist Pattern)
And Method For Manufacturing)
Semiconductor Device)
)
Confirmation No.: 3577)
)
Examiner: Brittany L. Raymond)
)
Art Unit: 1756)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT A

Applicants have the following response to the Office Action of December 7, 2006.

Please amend the above-identified application as follows: